



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification: H04L 25/02, H04L 25/49	A1	(11) International Publication Number: WO 00/16525 (43) International Publication Date: 23 March 2000 (23.03.2000)
(21) International Application Number: PCT/US99/20488		
(22) International Filing Date: 10 September 1999 (10.09.1999)		Published
(30) Priority Data: 60/099,770 10 September 1998 (10.09.1998) US		
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(54) Title: **A SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA SIGNALS OVER A CLOCK SIGNAL LINE**
 (54) Titre: **SYSTEME ET PROCEDE D'ENVOI ET DE RECEPTION DE SIGNAUX DE DONNEES PAR UNE LIGNE DE SIGNAL D'HORLOGE**

(57) Abstract

The system preferably includes a unique transmitter that sends both clock and data signals over the same transmission line. The receiver uses the same transmission line to send data signals back to the transmitter. The transmitter comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data from the clock signal. The receiver comprises a clock re-generator, a data decoder and a return channel encoder. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line. The return channel encoder generates signals and asserts them on the transmission line. The signal is asserted or superimposed over the clock and data signal provided by the transmitter.

(57) Abrégé

L'invention concerne un système comprenant de préférence un émetteur unique qui envoie des signaux d'horloge et de données par la même ligne de transmission. Le récepteur utilise la même ligne de transmission pour renvoyer des signaux de données à l'émetteur. L'émetteur comprend un générateur d'horloge, un décodeur et une interface de ligne. Le générateur d'horloge produit un signal d'horloge comprenant un flanc arrière à position variable. Le récepteur décode la position du flanc arrière pour extraire des données du signal d'horloge. Le récepteur comprend un re-générateur d'horloge, un décodeur de données et un codeur de canal retour. Le re-générateur d'horloge contrôle la ligne de transmission, reçoit des signaux, les filtre et génère dans le récepteur un signal d'horloge provenant du signal dans la ligne de transmission. Le codeur de canal retour génère des signaux et les active dans la ligne de transmission. Le signal est activé ou superposé au signal d'horloge et de données émis par l'émetteur.

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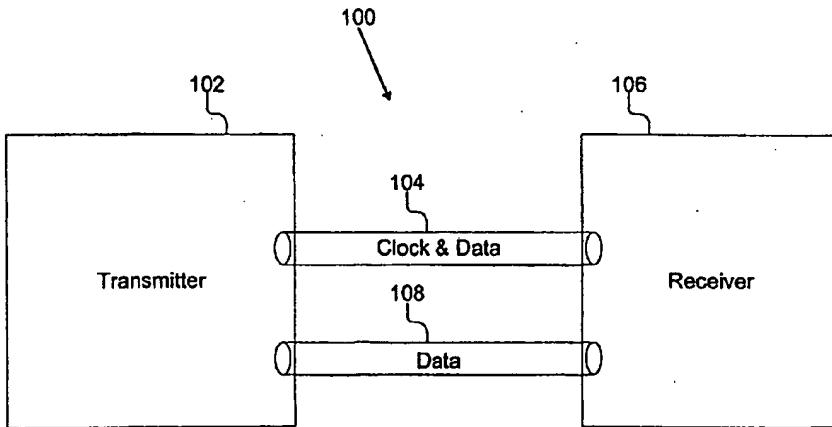
(51) International Patent Classification 7 : H04L 25/02, 25/49		A1	(11) International Publication Number: WO 00/16525
			(43) International Publication Date: 23 March 2000 (23.03.00)
(21) International Application Number: PCT/US99/20488		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 10 September 1999 (10.09.99)			
(30) Priority Data: 60/099,770 10 September 1998 (10.09.98) US Not furnished 9 September 1999 (09.09.99) US			
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Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: A SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA SIGNALS OVER A CLOCK SIGNAL LINE



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The system preferably includes a unique transmitter that sends both clock and data signals over the same transmission line. The receiver uses the same transmission line to send data signals back to the transmitter. The transmitter comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data from the clock signal. The receiver comprises a clock re-generator, a data decoder and a return channel encoder. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line. The return channel encoder generates signals and asserts them on the transmission line. The signal is asserted or superimposed over the clock and data signal provided by the transmitter.

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Description

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A System and Method For Sending and Receiving
Data Signals Over a Clock Signal Line

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Inventors: Gyudong Kim, Min-Kyu Kim & Seung Ho Hwang

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Cross-References To Related Applications

This application is a utility conversion of U.S. Patent No. 60/099,770, entitled "Embedded Back Channel For TMDS" by Gyudong Kim, filed September 10, 1998.

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BACKGROUND OF THE INVENTION

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1. Field of the Invention

The present invention relates generally to the field of data communications, and more particularly, to the transmission of clock and data signals. Still more particularly, the present invention relates to the transmission of clock signals and data signals on the same transmission line in transition minimized differential signaling (TMDS) system.

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20. Description of the Background Art

There are a variety of prior art systems and method for transmitting data between a transmitter and a receiver. Various serial links and other methods for transmitting data and clock signals are well known. However, most such schemes provide a single line or channel dedicated for the transmission of the clock signals and other signal lines or channels dedicated for the transmission of data. Once such system is described by Kyeongho Lee, Sungjoon Kim, Gijung Ahn, and Deog-kyoon Jeong in "A CMOS Serial Link For Fully Duplexed Data Communication," IEEE Journal of Solid State Circuits, Vol. 30, No. 4 pp. 353-364, April 1995.

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The present invention will be discussed in the context of transition minimized differential signaling (TMDS), however, those skilled in the art will recognize that the present invention is applicable in various other data communication contexts. In TMDS, four signal lines are provided, and each signal line is preferably a differential pair. One signal line

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5 is a for a low speed clock signal and the three other signal
lines are for high-speed data transmission.

10 One important aspect of all data communication systems is
to maximize the bandwidth provided by the data channels.

15 5 However, most systems include a variety of control signals that
must be sent between the transmitter and the receiver to ensure
proper operation, and maintain synchronization between the
transmitter and the receiver. For example, it is not uncommon
for as much as 20% of the bandwidth to be used for framing and
10 synchronization in serial communication. One problem is that
the bandwidth available for data is typically reduced because
the data signal lines must be used to transmit these control
signals between the transmitter and receiver. Yet another
20 problem is latency in transmitting the control signals to the
recipient. Especially in video data communication, much of the
data must be transmitted in blocks during which control signals
25 cannot be sent. For example, when transmitting data from a
controller to a flat panel, the data is transmitted, and then
there is a data enable period corresponding to the blanking
30 period in CRT display that is used to send control and
synchronization signal. Only during that data enable period can
the control signals be sent under most protocols. Therefore,
there is latency imposed on transmitting control signals to the
35 receiver. Thus, there is need for a system that can provide for
25 control signaling between the transmitter and the receiver
without decreasing the available bandwidth for data transfer,
and while reducing the latency in sending control signals.

40 Yet another problem in the prior art is that most systems
do not provide a mechanism to get signals from the receiver back
30 to the transmitter. In other words, there is not a return
channel for communication. Some systems have provided
45 additional signal lines, however, their addition and interface
add significant complication, require re-wiring and create other
problems that make the addition of a physical line unworkable.
35 Another approach is to add a second transmitter, second receiver
and signal lines. However, this essentially doubles the hardware

5 requirements making such a solution too expensive. Furthermore,
such duplication is overkill for the amount of data that needs
to be sent between the transmitter and the receiver, especially.
10 when the application is one of sending video data from a
transmitter to a receiver such as communication between a
5 graphic controller and a video display device.

15 Therefore, there is a need for a system and method for that
uses the clock signal line also for transmitting data signals
between the transmitter and the receiver and vice-versa.

10 SUMMARY OF THE INVENTION

20 The present invention overcomes the deficiencies and
limitations of the prior art with a unique data communication
system. The system preferably includes a unique transmitter and
receiver coupled by a transmission line. The transmitter sends
15 both a clock signal and data signals over the transmission line
to the receiver. The receiver uses the same transmission line
25 to send data signals back to the transmitter.

30 The transmitter preferably comprises a clock generator, a
decoder and a line interface. The clock generator produces a
20 clock signal that includes a variable position falling edge.
The falling edge position is decoded by the receiver to extract
data in addition to the clock signal. The line interface
35 couples the output of the clock generator to the transmission
line. The line interface also couples the transmission line to
25 the decoder and in doing so removes the signals from the clock
generator. The decoder receives the signals from the line
interface and decodes the signal to determine the data being
40 sent from the receiver to the transmitter on the same line used
to send the clock and data from the transmitter to the receiver.

30 The receiver preferably comprises a line interface, a clock
re-generator, a data decoder and a return channel encoder. The
45 clock re-generator, the data decoder and the return channel
encoder are coupled to the transmission line by the line
interface. The clock re-generator monitors the transmission
line, receives signals, filters them and generates a clock
50 35 signal at the receiver from the signal on the transmission line.

5 The data decoder similarly is coupled to receive the signals on
the transmission line, and filters and decodes the signals to
produce data signals. This is preferably done by determining
the position of the falling edge of the clock signal and
10 translating the falling edge position into bit values. In
contrast, the return channel encoder generates signals and
asserts them on the transmission line. These signals are
asserted or superimposed over the clock & data signals provided
15 by the transmitter.

10 These and other features and advantages of the present
invention may be better understood by considering the following
detailed description of a preferred embodiment of the invention.
20 In the course of this description, reference will frequently be
made to the attached drawings.

15 BRIEF DESCRIPTION OF THE DRAWINGS

25 Figure 1 is a block diagram of system including the
combined clock and data signal line of the present invention.

Figure 2 is a block diagram of a portion of the transmitter
showing a clock generator, decoder and a line interface.

30 Figure 3 is a block diagram of a preferred embodiment of
the clock generator constructed in accordance with the present
invention.

35 Figure 4 is a timing diagram illustrating various clock
signals that the clock generator of the present invention
25 produces.

40 Figure 5A is a block diagram of a preferred embodiment of
the line interface constructed in accordance with the present
invention.

45 Figure 5B is a circuit diagram of the preferred embodiment
30 of the line interface constructed in accordance with the present
invention.

50 Figure 6A is a block diagram of a first embodiment of the
decoder at the transmitter constructed in accordance with the
present invention.

Figure 6B is a block diagram of a second embodiment of the decoder at the transmitter constructed in accordance with the present invention.

Figure 7 is a block diagram of a first embodiment of portions of the receiver relating to the present invention.

Figure 8 is a block diagram of a first embodiment of a clock re-generator of the receiver.

Figure 9 is a block diagram of a preferred embodiment of a data decoder of the receiver.

10 Figure 10A is a block diagram of a first embodiment of a
return channel encoder of the receiver.

Figure 10B is a block diagram of a second and alternate embodiment of a return channel encoder of the receiver.

Figure 11A is a timing diagram illustrating signals on the transmission line, and the clock and data signals generated by the transmitter for return to zero signaling.

Figure 11B is a timing diagram illustrating signals on the transmission line, the data signal sent by the receiver, and the

clock and data signals recovered by the receiver for return to zero signaling.

Figure 12A is a timing diagram illustrating the timing of the data and clock signals on the transmission line, and the clock and data signals generated by the transmitter for non-return to zero signaling.

Figure 12B is a timing diagram illustrating signals on the transmission line, the data signal sent by the receiver, and the clock and data signals recovered by the receiver for non-return to zero signaling.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figure 1, a block diagram of system 100 including the combined clock and data signal line of the present invention is shown. The system 100 preferably includes a transmitter 102, a clock transmission line 104, a receiver 106 and one or more data transmission lines 108. The transmitter 102 preferably provides a clock signal as well as data signals to the receiver 106 via the clock transmission line 104. These data signals are in addition to those provided to the receiver

5 106 via the high speed data transmission lines 108. The
5 receiver 106 receives the signals on the transmission line 104
10 and from them, generates the clock and data signals at the
5 receiver 106. These data signals on the clock line 104 are
15 again in addition to the data signals that the receiver 106
recovered from the data transmission line 108. The transmitter
10 and the receiver 106 include logic for sending and receiving
the data from data transmission line 108. This logic preferably
15 includes transition control, DC balancing, and encoding/decoding
20 in a conventional manner. For example, in addition to the
components of the present invention for receiving and sending
data and clock signals on the clock transmission line 104 that
25 will be described below, the transmitter 102 and the receiver
15 respectively include conventional data transmission logic
for TMDS such as that provided in PanellLink by Silicon Image of
20 Cupertino, California. For ease of understanding that logic and
the data transmission line 108 are omitted from the discussion
25 below and the remaining figures. Those skilled in the art will
also realize that while shown as a single line, the clock
30 transmission line 104 and the data transmission line 108 are
preferably each a differential pair of signal lines, and the
signal is carried on the differential pair of lines.
35 Furthermore, those skilled in the art will understand the
preferred embodiment for the data transmission line 108 is three
25 pairs of data lines.

Transmitter

Referring now to Figure 2, a preferred embodiment of the transmitter 102 is shown in more detail. The transmitter 102 preferably comprises a clock generator 200, a line interface 204, and a decoder 202.

The clock generator 200 has a first input, a second input and an output. The clock generator 200 produces a clock signal that is encoded with data. The data is encoded into the clock signal by varying the modulation of the falling edge of the clock signal. In other words, the position of the falling edge of the clock relative to the rising edge indicates different

5 data values. This is particularly advantageous because it
preserves the rising edge of the clock for clock recovery. All
the activity for a bi-directional data link on the clock
transmission line 104 is centered around the falling edge of the
10 5 clock from the transmitter 102. While most of the present
invention will be described in the context of the falling edge
of the clock having two different positions, Figures 3 and 4
15 will also be described in the context of the falling edge of the
clock having five different positions. Each of the four
20 10 positions representing two bit values and one position
representing no data. The first input of the clock generator
200 is coupled to line 214 to receive a clock signal either from
another portion of the transmitter 102 or from a oscillator or
25 15 other conventional clock source. The second input of the clock
generator 200 is coupled to line 216 to receive control/data
signals. These control/data signals dictate the data or no data
that is transmitted as part of the clock signal. These
control/data signals may be from another portion of the
transmitter 102 or from off chip control logic. The output of
30 20 the clock generator 200 is provided on line 210 that is coupled
to an input of the line interface 204. The output of the clock
generator 200 provides a CGOut signal.

35 While the present invention is described throughout this
application as preserving the rising edge for the clock signal
40 25 and centering all the bi-directional data transmission about the
falling edge, those skilled in the art will realize that an
inverse scheme where the falling edge is preserved for
recovering the clock and changes in position of the rising edge
45 is used for encoding data is within the spirit and scope of the
30 present invention.

45 The line interface 204 has an input, an output and a bi-
directional port. The line interface 204 couples the clock
generator 200 and the decoder 202 to the clock transmission line
50 35 104. The input of the line interface 204 preferably couples line
210 to the clock transmission line 104 so that the CGOut signal
may be asserted over the clock transmission line 104. The

output of the line interface 204 is coupled to the input of the decoder 202 by line 212. The line interface 204 advantageously receives the signal on the clock transmission line 104, removes the CGOut signal as will be described below with reference to Figures 5A and 5B, and sends the filtered signal as the input to the decoder 202. The bi-directional port of the line interface 204 is coupled to the clock transmission line 104.

The decoder 202 receives the filtered signals from the transmission line 104 and decodes the signals to generate the data sent by the receiver 106. The decoder 202 preferably performs an inverse function to the encoder 704 (See Figure 7) of the receiver 106 as will be described below.

Referring now to Figures 3 and 4, the preferred embodiment for the clock generator 200 will be described. While the clock generator 200 will now be described as providing a clock signal having a falling edge in five possible locations to send two bits of data or no data in addition to the clock signal, those skilled in the art will recognize that this is only by way of example. The clock generator 200 could be configured to send from 1 to n bits of data per clock cycle depending on the clock frequency and the number of possible locations for the falling edge of the clock signal. In general, n locations of the falling edge will allow up to $\log_2 n$ bits of data to be transferred per clock cycle. The number of locations for the falling edge is limited only in that the first location must be such that the pulse width is greater than the logic-threshold crossing time of the rising edge, which may be viewed to be jitter by the phase-locked loop at the receiver 106. In other words, the thresholds for set up and hold time in the logic must be sufficient to recognize a rising edge as the beginning of the clock cycle.

The clock generator 200 preferably generates a clock signal at the dot clock frequency, or the frequency used by device (not shown) connected to the receiver 106 for the display of the data. The maximum symbol rate provided by data transfer as part of the clock signal matches the dot clock frequency. For

5 example, if the dot clock is 100 MHz, the symbol rate is 100
10 Msymbols/s. The actual data rate will depend on the modulation
methods and the number of bits per clock or symbol that can
sent. If simple binary modulation is used, then the bit rate is
15 the same and the clock rate with would provide an additional
10 100Mb/s for control signals.

20 The clock generator 200 preferably comprises a monostable
25 multivibrator 306, a delay-locked loop 300, a multiplexer 302, a
30 first NAND gate 304 and a second NAND gate 306. The clock
35 generator 200 preferably uses only return to zero signaling for
40 sending the clock and data signals. Non-return to zero
45 signaling cannot be used for sending from the transmitter 102.
50 The clock signal is received on line 214 and provided as input
55 to the input of the one shot or monostable multivibrator 306.
60 The monostable multivibrator 306 is provided to generate a
65 signal with a narrower pulse width than the clock signal. This
70 signal is advantageous for use in other portions of the clock generator
75 200. In an alternated embodiment, the one shot 306, may be
80 replaced by a plurality of monostable multivibrators each
85 respectively coupled in series with an output signal line 308 of
90 the delay locked loop 300. Such an alternate embodiment
95 provides more flexibility in the design of the delay locked loop
100 300 at the cost of additional monostable multivibrator as will
105 be understood by those skilled in the art. The output of the
110 monostable multivibrator 306 is coupled to the input to the
115 delay-locked loop 300. The delay-locked loop 300 is of a
120 conventional type and in response to a signal at its input,
125 provides a plurality of outputs, each output being the same as
130 the input only shifted in phase. The falling edge is modulated
135 using a delay-locked loop 300. The falling edge is chosen from
140 one of the phases provided by the delay-locked loop 300. It is
145 preferable that the selected phases from the delay-locked loop
150 300 be the ones close to a 50% duty cycle. The delay-locked
155 loop 300 preferably provides five output signals: ϕ_0 , ϕ_1 , ϕ_2 ,
160 ϕ_3 , ϕ_4 , and ϕ_n . The ϕ_0 signal is the clock signal unchanged.
165 The ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 , and ϕ_n are each phase shifted more with

5 respect to the previous ϕ signal. The ϕ_0 is coupled to a first
input of the first NAND gate 304. The output of the first NAND
gate 304 is provided on line 210 and provides the CGOut signal.
The first NAND gate 304 is cross coupled with the second NAND
gate 306 to form a set-reset latch. A rising edge on the ϕ_0
10 causes the output of first NAND gate 304 to be set high or
asserted until reset to low by the second NAND gate 306. The
remaining signals from the delay-locked loop 300, ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 ,
15 and ϕ_n are coupled to respective data inputs of the multiplexer
10 302. The control input of the multiplexer 302 is coupled to
line 216 to receive control/data signals. In response to the
control/data signals on line 216, the multiplexer 302 will
couple one of the signals from the delay-locked loop 300, ϕ_1 ,
20 ϕ_2 , ϕ_3 , ϕ_4 , and ϕ_n , to the input of the second NAND gate 306.
25 Thus, the rising edge on the selected signal from the delay-
locked loop 300, ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 , and ϕ_n , will cause the latch to
be reset and create a falling edge on the output of the first
NAND gate 304, and thus, line 210. Thus, it is apparent that
30 using the control/data signals to select one of the signals, the
position of the falling edge can be selected. For example
control signals such as shown in Table I may be used to control
the position of the falling edge.

Control/data Signal(216)	NAND-gate 306 input	Falling edge Position	Data Sent
000	ϕ_1	T0	00
001	ϕ_2	T1	01
100	ϕ_3	T2	00
010	ϕ_4	T3	10
011	ϕ_n	T4	11

Table I

45 Those skilled in the art will recognize how the clock generator
200 could be modified to create any number of different falling
50 25 edge positions for the CGOut signal. Referring also to Figure

5 4, a timing diagram of the clock/ ϕ_0 , ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 , and ϕ_n and
10 the possible CGOut signals are shown. There are five possible
15 CGOut signals. First, the clock/ ϕ_0 signal is unchanged which is
20 the input signal with falling edge at time T2 and sending
25 no data. The remaining CGOut1-CGOut4 signals are have a falling
30 edge with an adjusted position to times T0, T1, T3, T4
35 respectively each representing a different two bit value. Thus,
40 the preferred embodiment is able to transfer two bits per clock
45 from the transmitter 102 to the receiver 106 in addition to the
clock signal. Since the receiver 106 uses only the rising edge
50 to detect and define clock cycles, the present invention uses
55 this to achieve the data transfer without any performance
disadvantages. For the receiver 106 embodiments described below
60 where only one bit of data per clock is sent, the clock
65 generator 200 would output falling edges at times T1 and T3.

25 The ability of the present invention to use the clock
transmission line 104 to send data from the transmitter 102 to
the receiver 104 is particularly advantageous because it
30 eliminates signal latency present in the prior art. With the
35 present invention as applied to TMDS, the transmitter 102 does
40 not need to wait for the next available data enable (DE) low
45 period to send the signals. This greatly decreases the maximum
50 transfer latency. Moreover, the present invention can be used
55 in other serial links that require very short latency. For
60 example, if a fixed bit location is assigned for each link (a
65 fixed bandwidth per fixed dot clock) the synchronization
70 overhead for those channels can be minimized. In this way, the
75 latency of such links can be reduced to 1 frame cycle and the
80 cable flight time. The other bits of the payload can be used
85 with variable bandwidth but the synchronization latency or delay
90 could be longer.

45 Yet another advantage of the forward channel for sending
data from the transmitter 102 to the receiver 106 is that it is
50 fully backward compatible with prior TMDS designs and protocols.
55 Thus, whether the receiver 106 is able to receive data from the
60 transmitter 102 or not, the clock signal is unaffected by the
65

5 addition of data to the signal. Moreover, a receiver 106 will
not have problem recovering the clock even if data (for either
the transmitter 102 or the receiver 106) is added in accordance
10 with the present invention to the signal on the transmission
line 104. Therefore, the transmitter 102 of the present
5 invention can still be used even if the receiver does not have
the capability to receive the data signal.

15 Referring now to Figure 5A and 5B, the preferred embodiment
for the line interface 204 is shown. The line interface
10 preferably comprises a first amplifier 502, a second amplifier
506, a differential amplifier 504 and a line terminator or pull-
20 508, a differential amplifier 504 and a line terminator or pull-
up resistor 508. The line interface 204 is essentially a bi-
directional bridge that allows transmission of data while
receiving data from the receiver 106. The input of the first
25 15 amplifier 502 is coupled to line 210 to receive the CGOut
signal. The input of the second amplifier 506 is similarly
coupled. The output of the first amplifier 502 is coupled to
apply an amplified version of the CGOut signal to clock
30 transmission line 104. The clock transmission line 104 is also
coupled by the pull-up resistor 508 to high voltage to form a
20 line terminator. The pull-up resistor 508 could instead be
coupled to ground or half V_{DD} as will be understood to those
skilled in the art for alternate embodiments of the line
35 35 terminator. The clock transmission line 104 is also coupled an
input of the differential amplifier 504. The other input of the
25 differential amplifier 504 is coupled to the output of the
differential amplifier 504. The second amplifier 506 also receives
40 the CGOut signal and amplifies the signal, but to the same or
lesser extent than the first amplifier 502. The differential
30 amplifier 504 subtracts the CGOut signal from the signal
received from the clock transmission line 104. Thus, the output
45 of the differential amplifier 504 that is provided on line 212
includes predominately the signals asserted by the receiver 106
50 on the clock transmission line 104 and not the CGOut signal. It
35 should be noted that an identical circuit with inputs and output

5 coupled differently may also be used in the receiver 106 as will
be described below with reference to Figure 7.

10 Referring also now to Figure 5B, a circuit diagram for one
15 exemplary embodiment for the line interface 204 is shown. The
connections to the signal lines 210 and 104 are shown with
20 reference numerals for clarity and ease of understanding. The
signals preferably use differential pairs are indicated by
25 reference numerals "a" and "b" as will be understood to those
skilled in the art. The transistors and other components
30 forming the second amplifier 506 and the differential amplifier
504 are shown grouped within dashed boxes as will be understood
35 to those skilled in the art. The remaining transistors and
other components from the first amplifier (not labeled in Figure
40 5B). It should be noted that some of the transistors in the
45 second amplifier 506 are for impedance matching, and have their
50 gates coupled to signal line 522 to be biased for impedance
55 matching in a conventional manner. Some of the transistors in
the differential amplifier 504 are also coupled to line 520 for
60 biasing. In alternate embodiments, the outputs of the
65 differential amplifier 504 could be coupled to line 520 and
70 thereby provide a single output signal as will be realized by
75 those skilled in the art. Those skilled in the art will further
80 recognize that in alternative embodiments, various other
85 conventional bi-directional buffers could be used in place of
90 the circuits shown in Figures 5A and 5B.

95 Referring now to Figures 6A and 6B, two alternate
100 embodiments for the decoder 202 are shown. The embodiment for
105 the decoder 202 is dependent on the type of signaling being used
110 by the corresponding encoder 704 (See Figure 7 and below) in the
115 receiver 106. Figure 6A shows a block diagram of the first
120 embodiment of the decoder 202a at the transmitter 106 for use
125 when the receiver 106 sends the data in a non-return to zero
130 (NRZ) signaling. As shown in Figure 6A, when the receiver 106
135 sends data in NRZ (non-return to zero) manner and toggles data
140 at the fictitious falling edge (since the clock toggles its
145 falling edge randomly in accordance with the present invention),

5 since the delay is a function of cable delay, at the transmitter
side, it is not predictable where the relative location of the
10 data transition will be, even though it may have been obvious
at the receiver side. Because of this ambiguous delay, the
5 decoder 202a oversamples the data provided from the clock
transmission line 104/212. Since the incoming data rate is the
15 same as outgoing data rate, the present invention generates
multiple phases of clocks from the clock signal on line 214.
Using these clocks, the signal line 212 is sampled multiple
10 times per data period to locate a data transition. Once the
transition is detected, it is used as the data boundary.

20 As shown in Figure 6A, the first embodiment of the decoder
202a preferably comprises a delay-locked loop 602, a sampling
unit 604, a data generator and a transition detector 608. The
15 delay-locked loop 602 has an input coupled to receive the clock
signal on line 214. The same delay-locked loop could be used in
25 both the clock generator 200 and the decoder 202. The delay-
locked loop 602 is of a conventional type and provides a
plurality of versions of the clock signal phase shifted. Outputs
30 of the delay-locked loop 602 are coupled to respective inputs of
the sampling unit 604. The sampling unit 604 includes control
logic for generating a signal on a first output that controls
35 when the transition detector 608 samples and latches the signal
on line 212. For example, the sampling unit 604 can generate
25 this control signal for every rising edge seen at the input from
the delay-locked loop 602. The first output is coupled to an
input of the transition detector 608. The sampling unit 604
40 also provides a time signal on a second output indicating the
signals from the delay-locked loop 602 that have transitioned,
30 and thus, the time within the clock cycle. The second output of
the sampling detector 604 is coupled to an input of the data
45 generator 606. The transition detector 608 has an input coupled
to line 212 to receive the signal from the receiver 106. The
transition detector 608 detects transitions in the signals on
35 the line 212. When a transition is present the transition
detector 608 asserts its output. The data generator 606 is
50

5 coupled to the sampling unit 604 to receive a signal indicating
the time within the clock cycle and the transition detector 608
10 to identify when the transition occurs. Using this information,
the data generator 606 outputs the bit values corresponding to
15 when the transitions occur. For example if the transition is
before the time for a falling edge of the clock if it had a 50%
duty cycle then the data generator 606 may output a 1 if after
the data generator 606 could output a 0 if the data rate were
20 one bit per clock cycle. Those skilled in the art will
recognize how the data generator 606 could be modified according
to the number of bits per clock cycle transmitted by the
receiver 106. The output of the data generator 606 is provided
on line 218 for use by the transmitter 102.

Figure 6B shows an alternate embodiment for the decoder
202a. When receiver 106 sends data in return to zero (RZ)
25 manner, the rising edge of the incoming clock is preferably used
as the data reference point, and a phase in the middle of those
consecutive rising edges is generated and used to sample the
30 incoming data at that point. Thus, the decoder 202a comprises
merely a delay-locked loop 650 and a flip-flop 620. The delay-
locked loop 650 preferably provides a signal that has a rising
edge in about the middle of the clock cycle such as #3. This
35 signal is coupled to the clock input of the flip-flop 620 to
cause the flip-flop 620 to latch near the middle of the clock
cycle. The data input of the flip-flop 620 is coupled to line
40 212 to receive the data signal sent by the receiver 106 and the
D output of the flip-flop 620 provides the data output and is
coupled to line 218.

Those skilled in the art will recognize that the decoder
202 may alternatively formed as an integrator type receiver
45 where the period of the clock is subdivided and the integrator
integrates over the subdivided time periods and compares the
integration results. The signal is effectively integrated and
dumped for comparison to determine the data values.

50 35 Receiver

Figure 7 shows a preferred embodiment for the receiver 106 constructed in accordance with the present invention. The receiver 106 preferably comprises a line interface 706, a clock re-generator 700, a data decoder 702, a delay compensator 708 and a return channel encoder 704.

The line interface 706 is preferably identical to that described above with reference to Figure 5A and 5B. However, for the receiver 106, the line interface 706 is completely optional and the receiver 106 can operate without it. The line interface 706 buffers the signals and filters them for better use in recovery. The line interface 706 has an input, an output and a bi-directional port. The bi-directional port is coupled to the clock transmission line 104. The input of the line interface 706 is coupled to line 720 to receive the output of the return channel encoder 704. The output of the line interface 706 is coupled to line 722 to provide input signals to the clock re-generator 700 and the data decoder 702. For ease of understanding reference numerals for the line interface 706 have been added to Figure 5A.

The clock re-generator 700 has an input and an output. The input of the clock re-generator 700 is coupled to receive the signals on the clock transmission line 104 via line 722 from the line interface 706. The clock re-generator 700 monitors the transmission line 104, receives signals, filters them and generates a clock signal at the receiver 106. The output of the clock re-generator 700 is coupled to line 710 and provides the clock signal for the receiver 106 to use in recovering data from the data channels 108. The clock re-generator 700 advantageously only uses the rising edges of the signals on the transmission line 104 to regenerate the clock signal at the receiver 106. This allows the falling edge position and voltage level to be used for other data transfer. The preferred embodiment for the clock re-generator 700 is simply an amplifier that can provide an amplified version of the signal to other digital logic receiving the clock. Referring now also to Figure 8, another embodiment for the clock re-generator 700 is shown.

5 In Figure 8, the clock re-generator 700 is a phase-locked loop
800 that has an input that is coupled to the transmission line
104 and an output that provides the clock as a square wave. The
phase-locked loop 800 is a conventional type and includes a
10 5 phase detector 802, an amplifier and filter 804 and a voltage
controlled oscillator 806. These components 802, 804, 806 are
coupled in a conventional manner with the input of the phase
15 detector 802 coupled to line 104 and the output of the voltage
controlled oscillator providing the clock signal and being feed
10 back to the phase detector 802. Those skilled in the art will
recognize that various other embodiments of phase-locked loops
could be used for the clock re-generator 700 since it is only
20 necessary to detect the rising edges on the transmission line
104 and produce a clock signal therefrom. Alternate embodiments
15 for the clock re-generator 700 could also use a delay-locked
loop.

25 The data decoder 702, like the clock re-generator 700, has
an input coupled to receive the signals on the transmission line
104 via line 722 from the line interface 706. The data decoder
20 702 filters and decodes the signals to produce data signals that
are output on line 712. The data decoder 702 also has another
input coupled to line 710 to receive the recovered clock signal
from the clock re-generator 700. This is preferably done by
30 25 determining the position of the falling edge of the clock signal
and translating the falling edge position into bit values. The
data being sent from the transmitter 102 to the receiver 106 is
valid on the falling edge of the clock. Referring also now to
35 30 Figure 9, a preferred embodiment for the data decoder 702 will
be discussed. The preferred embodiment of the data decoder 702
is very similar to the second embodiment of the decoder 202b of
the transmitter 102. The data decoder 702 differs only in its
40 35 coupling to other components which is shown in Figure 9. The
data decoder 702 includes a delay-locked loop 650 and a flip-
flop 620. The clock input of the delay-locked loop 650 is
coupled to line 710 to receive the regenerated clock signal.
45 50 The data input to the flip-flop 620 is coupled to line 722 to

5 receive the filter data signals from the transmission line 104. The output of the flip-flop 620 provides the data output and is coupled to line 712. The operation is same as has been described above with reference to Figure 6B.

10 5 The delay compensator 708 is coupled to line 710 to receive the recovered clock signal. The delay compensator 708 adjusts the recovered clock signal to compensate for propagation delay over the transmission line 104 and propagation delay in recovering the clock such that the signal used to time the 15 10 sending of data back to the transmitter 102 will have timing that matches the original clock signal on the transmitter side of the clock transmission line 104. The output of the delay compensator 708 provides an adjusted clock signal and is used by the return channel encoder 704. In a preferred embodiment, the 20 15 delay compensator 708 is a phase-locked loop with a delay circuit in the feedback loop between the voltage-controlled oscillator and the phase detector, as will be understood to those skilled in the art. Such a configuration provides negative delay so that the clock signal for return channel 25 20 signals is moved ahead so that with propagation delay it will matches the timing of the CGOut signal at the transmitter 102.

30 The return channel encoder 704 generates signals and asserts them on the transmission line 104 via line 720 and the line interface 706. The return channel encoder 704 has a data 35 25 input coupled to line 714 to receive the control and data signals to for the data to be sent on the return channel. The return channel encoder 704 also has a clock input coupled by line 724 to the output of the delay compensator 708 to receive a modified clock signal for timing the assertion of data and 40 30 change in data states. These signals are asserted or superimposed over the clock & data signals provided by the transmitter 102. The return channel encoder 704 advantageously 45 sends data back to the transmitter 106 on the falling edge of the clock thereby preventing the return channel 704 from causing 50 35 any jitter on the clock signal. More specifically, the return channel encoder 704 minimizes transition activity only around

5 the rising edge of the clock, and minimizes activity by fixing
the polarity around the rising edge. This is accomplished by
including a delay-locked loop in the return channel encoder 704.
The return channel encoder 704 advantageously places data on the
10 transmission line 104 or clock pair in the form of voltage
signal and not edge position, thus reducing any interference and
effect on the transmission of the clock and data signals by the
transmitter 102.

15 Referring now to Figure 10A, a first embodiment of the
10 return channel encoder 704a is shown. The first embodiment
return channel encoder 704a provides the minimum functionality
for transmission. For example, the return channel encoder 704a
20 could be a 1-bit link. This has a low data rate and does not
allow DC balancing, however it is advantageous because there is
15 no latency (once the data is at the transmitter there is no
latency due to decoding) in getting the data and it is simple to
25 implement. The first embodiment of the return channel encoder
704a includes a rising edge detector 1002, a delay circuit 1004
and a latch 1008. The rising edge detector 1002 has an input
30 coupled to line 724 to receive a signal for timing the changing
of the data output. The rising edge detector 1002 detects the
rising edge and then asserts its output upon receiving rising
35 edge. The output of the rising edge detector 1002 is coupled to
the input of a delay circuit 1004. The delay circuit delays the
signal output of the rising edge detector 1002, such as by half
40 the clock period. Thus, the output of the delay circuit 1004 is
at a time of an ideal falling edge if the clock were to have a
50% duty cycle. The output of the delay circuit 1004 is used to
control or latch the latch 1008. Thus, the data will only
45 change state on an ideal falling edge of the input timing signal
30 on line 724. The latch 1008 also has a data input and a data
output. The data input is coupled to line 714 to receive the
data, and the data output is coupled to line 720 for assertion
55 by the line interface 706. Those skilled in the art will
understand how to construct other return channel encoders such

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5 as when more than one bit is send back to the transmitter 102 per clock cycle.

10 Furthermore, those skilled in the art will realize that the rising edge detector 1002 and the delay circuit 1004 may be 15 replaced by a delay-locked loop or a phase-locked loop as will now be discussed with reference to Figure 10B. Referring now to Figure 10B, a second embodiment of the return channel encoder 704b is shown. The second embodiment of the return channel encoder 704b includes a delayed locked loop 650 and a flip-flop 20 620. This is identical in operation to Figure 6B, and it 25 operation has been described above. The input to the delayed locked loop 650 is coupled to line 724 and the data input of the flip-flop 620 is coupled to line 714. The data output of the 30 flip-flop 620 provides the data output on line 720.

35 It should be understood that the either embodiment of the 25 return channel encoder 704a, 704b could also include an encoder for providing encoding of the data before transmission over the 30 return channel. The addition of an encoder such as 4bit/5bit encoder or a 9bit/10bit encoder is advantageous because it increases the amount of data that can be sent per clock cycle. 35 It also provides DC balancing and transition control. However, it makes the transmitter and receiver designs more complicated and adds latency to the availability of the data.

40 Referring now to Figures 11A, 11B, 12A, and 12B, timing 45 diagrams for the key signals of the present invention are shown. The timing diagram includes: 1) the CGOut signal on line 210 which is asserted on the clock transmission line 104; 2) the 50 signal on the clock transmission line 104; 3) the re-generated clock signal on line 710; 4) the recovered data signal on line 712; and 5) the return channel signal asserted by the return channel encoder 704 on the clock transmission line 104. Figure 11A illustrates the signals at the transmitter 102 using a return to zero signaling method. Similarly, Figure 11B 55 illustrates signals on the transmission line, and signal in the receiver 106 using a return to zero signaling method. In contrast, Figures 12A and 12B show the signal relationships for

5 a non-return to zero signaling method. Figure 12A shows the
signals at the transmitter 102 and Figure 12B shows the signals
at the receiver 106.

10 These timing diagrams demonstrate a number of features of
5 the combined clock and bi-directional data link of the present
invention. First, that transition activity and polarity
activity by either the transmitter 102 or the receiver 106 is
15 minimized or eliminated close to the rising edge of the CGOut
signal. Second, the transmission of data from the transmitter
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10 102 to the receiver 106 is through the position of the falling
edge of the clock signal. Third, the transmission of data from
the receiver 106 to the transmitter 102 is by current or voltage
20 level adjustment and any changes are not made near the rising
edge of the clock signal from the transmitter 102. Fourth, the
15 effect of assertion of data signals by the receiver 106 does not
impact the edges in the signals from the transmitter 102.

25 Clock Multiplication

One important advantage of the present invention is that no
modification to any portions of the present invention need to be
30 changed to be operable with or without clock multiplication. In
some cases, the transmitter 102 and the receiver 106 have the
ability to increase the data transmission rate by increasing the
clock rate through clock multiplication (sending multiple clock
35 signals within one period of the clock signal). In such a case,
25 the transmitter 102 asks the receiver 106 if it can handle clock
multiplication. The receiver 106 indicates to the transmitter 102
what if any levels of clock multiplication can be handled. The
transmitter then sends on the highest clock multiplication level
40 possible. In clock multiplication, the transmitter 106 just sends
30 a multiplied clock, however, the receiver 106 has to divide that
multiplied clock down to the original pixel clock so that the main
data channel can make use of the clock. The phase information on
the clock is also important in some data links and it can also be
45 conveyed through the data link provided with the present
35 invention. In the transmitter 102, a DLL/PLL is used to multiply
50 the clock at the integer multiple of the incoming clock. For some

5 transmission lines, since the jitter information is important, only integer multiple is allowed. However, if this is not that important, rational number multiples can also be used to save the bandwidth.

10 It is to be understood that the specific mechanisms and techniques that have been described are merely illustrative of one application of the principles of the invention. Numerous additional modifications may be made to the apparatus described 15 above without departing from the true spirit of the invention.

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WHAT IS CLAIMED IS:

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1. An apparatus for transmitting a clock signal and data signals over a signal line, the apparatus comprising a clock generator having a first input, a second input and an output, the clock generator modulating a falling edge of an output signal to indicate different data values, the first input of the clock generator coupled to receive a clock signal, and the second input of the clock generator coupled to receive a control signal indicating a data value to be transmitted.

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2. The apparatus of claim 1, further comprising a data decoder for extracting data signals, the data decoder having a input and an output, the data decoder for extracting data signals, the input of the data decoder coupled to the signal line, the output providing data from the signal line.

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3. The apparatus of claim 2, further comprising a line interface for asserting signals on and extracting signals from the signal line, the line interface having an input, an output and a bi-directional port, the bi-directional port coupled to the signal line, the input of the line interface coupled to the output of the clock generator, the output of the line interface coupled to the input of the decoder.

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4. The apparatus of claim 3, wherein the line interface further comprises a first amplifier coupling the output of the clock generator to the signal line, a differential amplifier having a first input coupled to the signal line, a second amplifier coupling the clock generator to a second input of the differential amplifier, and the output of the differential amplifier providing the output of the line interface.

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5. The apparatus of claim 1, wherein the clock generator further comprises:
50 a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from

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an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a multiplexer having a plurality of inputs and an output for selecting one of the plurality of input signals for output, the plurality of inputs of the multiplexer coupled to respective outputs of the delay-locked loop; and

a latch having a first input and a second input, the first input coupled to an output of the delay-locked loop, and the second input coupled to output of the multiplexer.

20 6. The apparatus of claim 5, further comprising a
monostable multivibrator having an input and an output, the
input of the monostable multivibrator to receive the clock
15 signal, the output of the monostable multivibrator coupled to
the input of the delay locked loop.

7. The apparatus of claim 5, wherein the latch further comprising a pair of cross coupled NAND gates.

8. The apparatus of claim 2, wherein the decoder further
20 comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a sampling unit having a plurality of inputs, a first output and a second output, the sampling unit for controlling when signals are sampled and for indicating the time at which signals are sampled, the plurality of inputs coupled to respective outputs of the delay-locked loop;

a transition detector for determining when there is a transition in a signal, the transition detector having a data input, a control input and a data output, the

data input of the transition detector coupled to the signal line, the control input of the transition detector coupled to the first output of the sampling unit; and

a data generator having a first input, a second input and an output, data generator for producing bit values corresponding to when transitions occur on the signal line, the first input of the data generator coupled to the second output of the sampling unit, the second input of the data generator coupled to the output of the transition detector.

9. The apparatus of claim 2, wherein the decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

10. The apparatus of claim 1, wherein the apparatus is coupled by the signal line to a receiver, and wherein the receiver further comprises:

a clock re-generator having an input and an output for recovering a clock signal from the signal line, the input of the clock re-generator coupled to the signal line;

a second decoder for extracting data signals, the second decoder having a first input, a second input and an output, the second decoder for extracting data signals, the first input of the second decoder coupled to the signal line, the second input of the second

5 generator and the output providing data from the signal line.

10 11. The apparatus of claim 10, wherein the clock re-
5 generator of the receiver is an amplifier.

12. The apparatus of claim 10, wherein the clock re-generator of the receiver is an phase-locked loop.

13. The apparatus of claim 10, wherein the second decoder further comprises

20 10 a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to output of the clock re-generator;

25 a sampling unit having a plurality of inputs, a first
15 output and a second output, the sampling unit for
controlling when signals are sampled and for
indicating the time at which signals are sampled,
30 plurality of inputs coupled to respective outputs
the delay-locked loop;

5 14. The apparatus of claim 10, wherein the second decoder
further comprises

10 a delay-locked loop having an input and a plurality of
outputs for outputting signals shifted in phase from
an input signal, the input of the delay-locked loop
coupled to the output of the clock re-generator;

15 a flip-flop having an control input, a data input and an
output, the control input of flip-flop coupled to one
of the plurality of outputs of the delay-locked loop,
and the data input of the flip-flop coupled to the
signal line.

20 15. The apparatus of claim 10, further comprising a second
line interface for asserting signals on and extracting signals
from the signal line, the second line interface having an input,
15 an output and a bi-directional port, the bi-directional port
coupled to the signal line, the output of the line interface
coupled to the input of the second decoder and the clock re-
generator.

25 16. The apparatus of claim 10, further comprising a delay
compensator having an input and an output for adjusting a
recovered clock signal to compensate for propagation delay, the
input of the delay compensator coupled to the output of the
clock re-generator.

30 17. The apparatus of claim 16, further comprising a return
channel encoder having a first input, a second input and an
output, for sending signals on the signal line, the first input
40 of the return channel encoder coupled to receive data for
transmission, the second input of the return channel encoder
coupled to the output of the delay compensator, and the output
35 of the return channel encoder coupled to the signal line.

45 18. The apparatus of claim 17, wherein the return channel
encoder further comprises:

50 a delay-locked loop having an input and a plurality of
outputs for outputting signals shifted in phase from

an input signal, the input of the delay-locked loop coupled to the output of the delay compensator;

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

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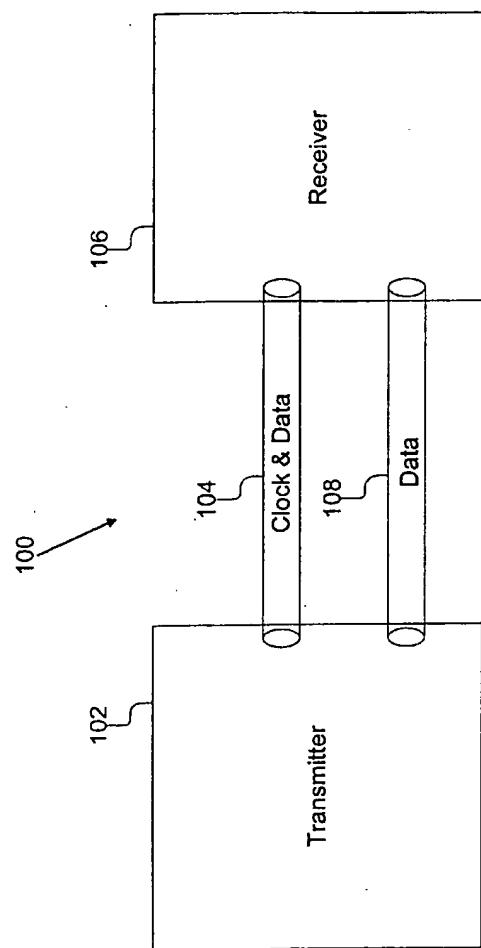


Figure 1

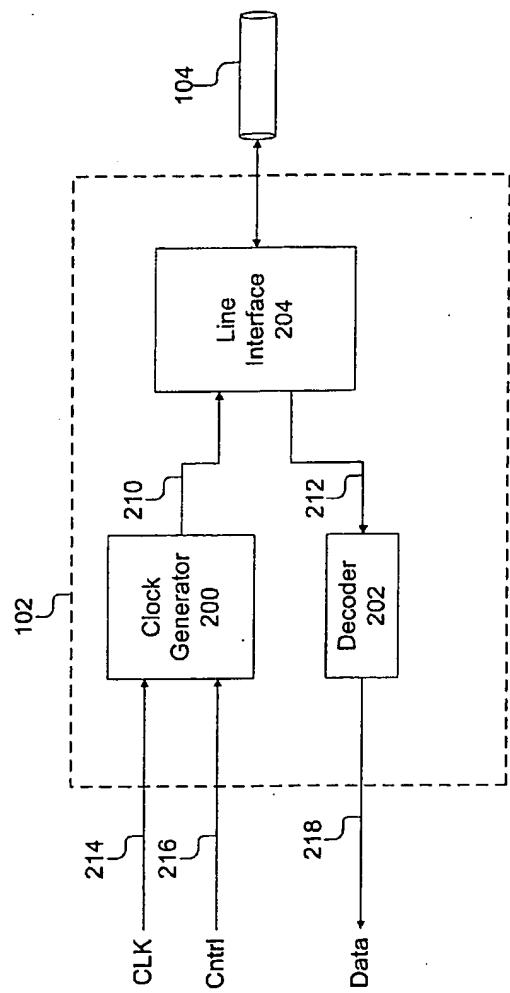


Figure 2

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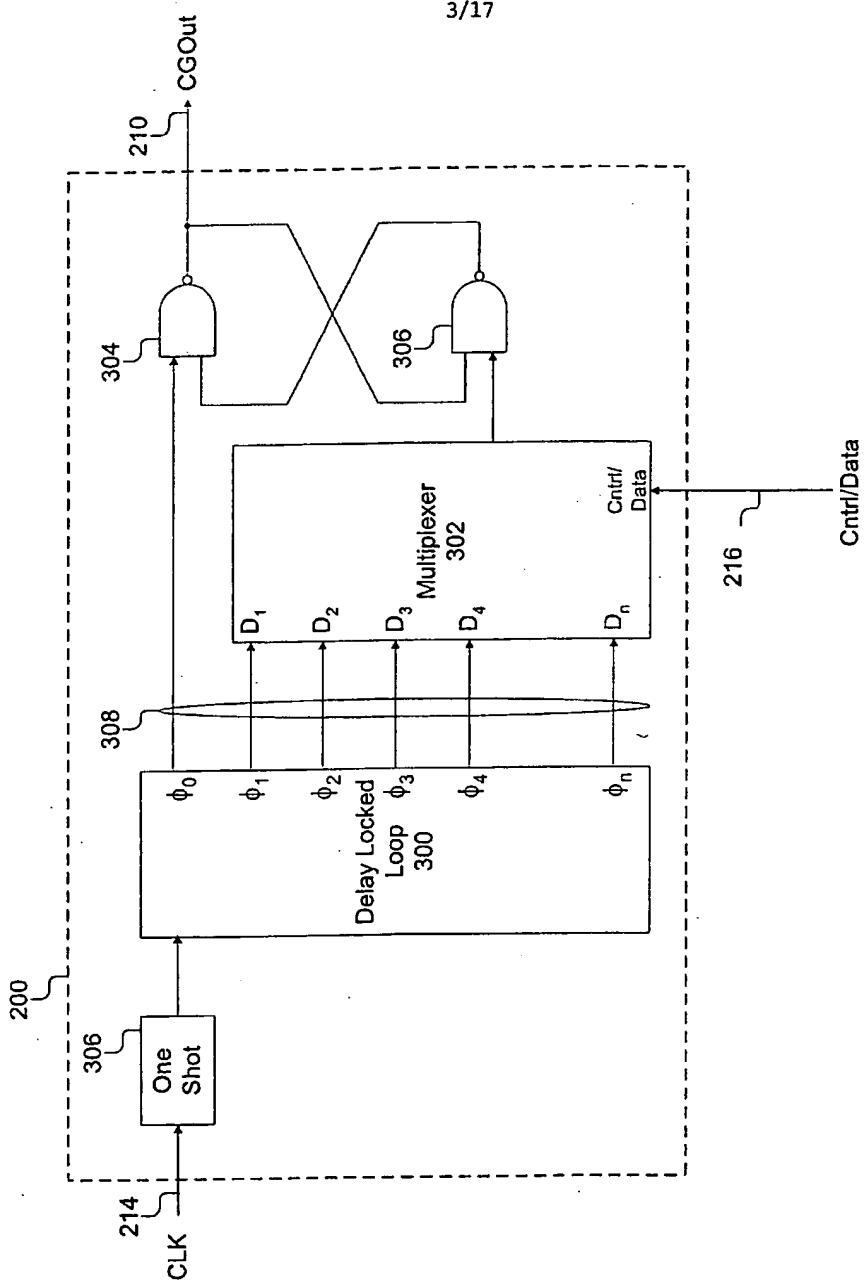
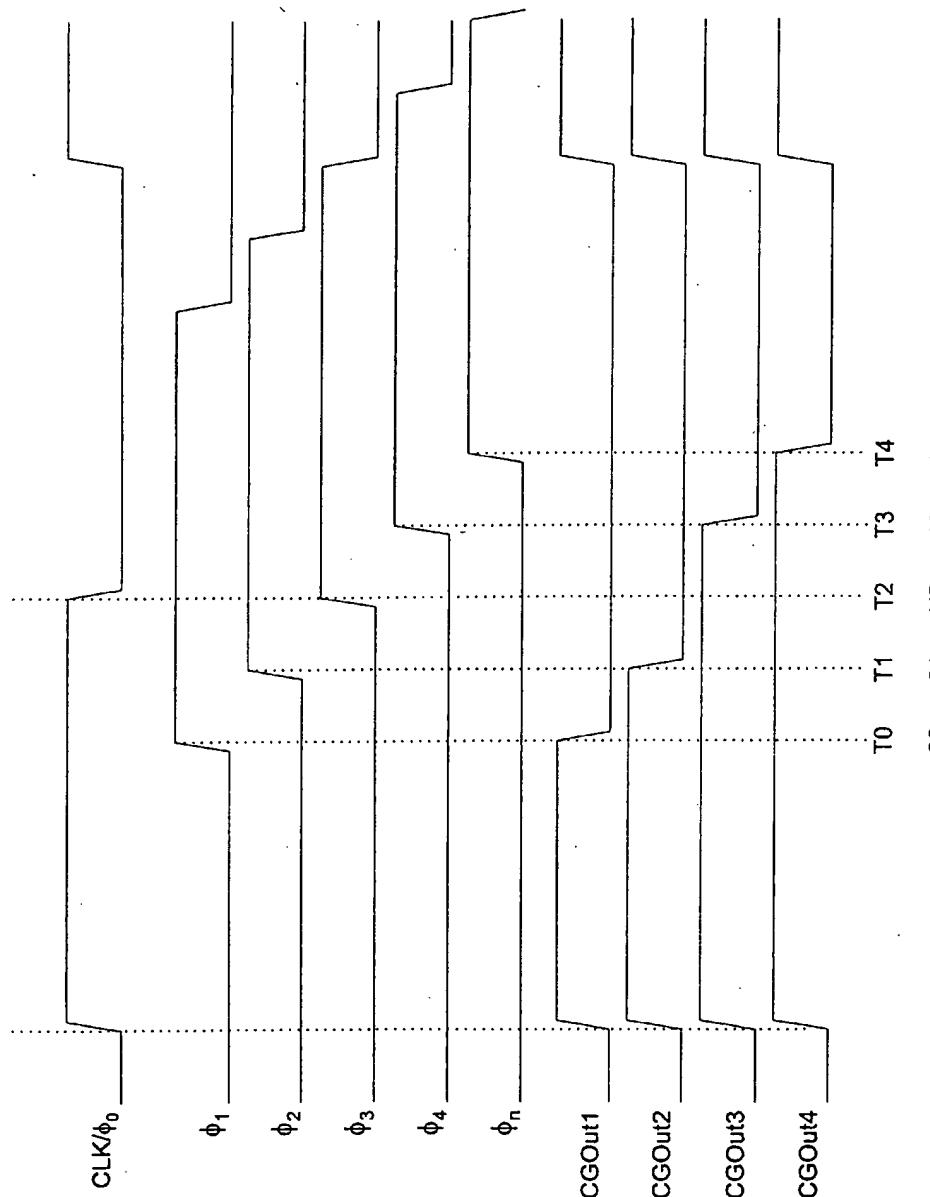


Figure 3

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**Figure 4**

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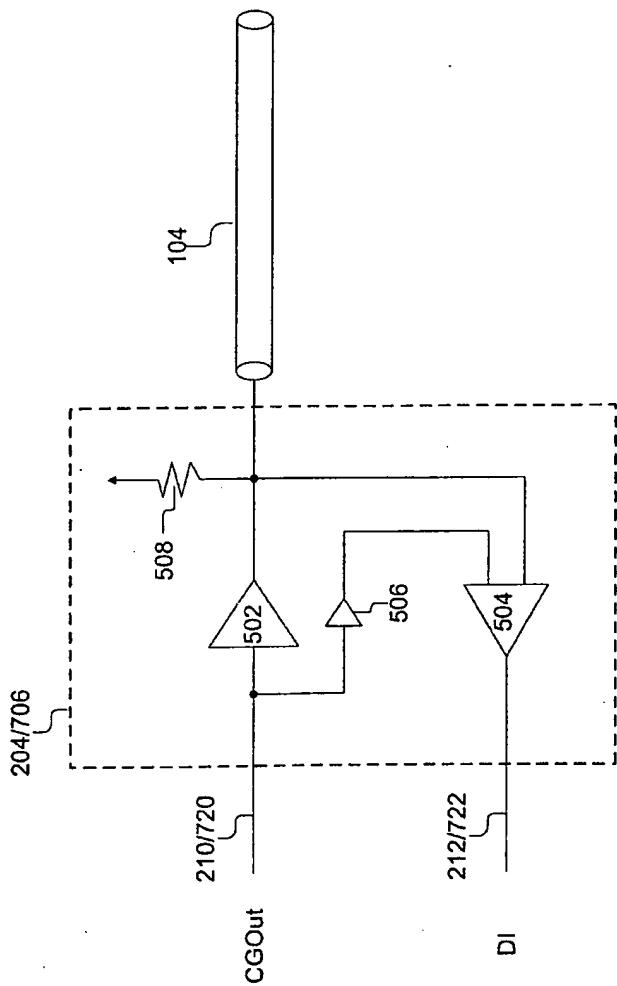


Figure 5A

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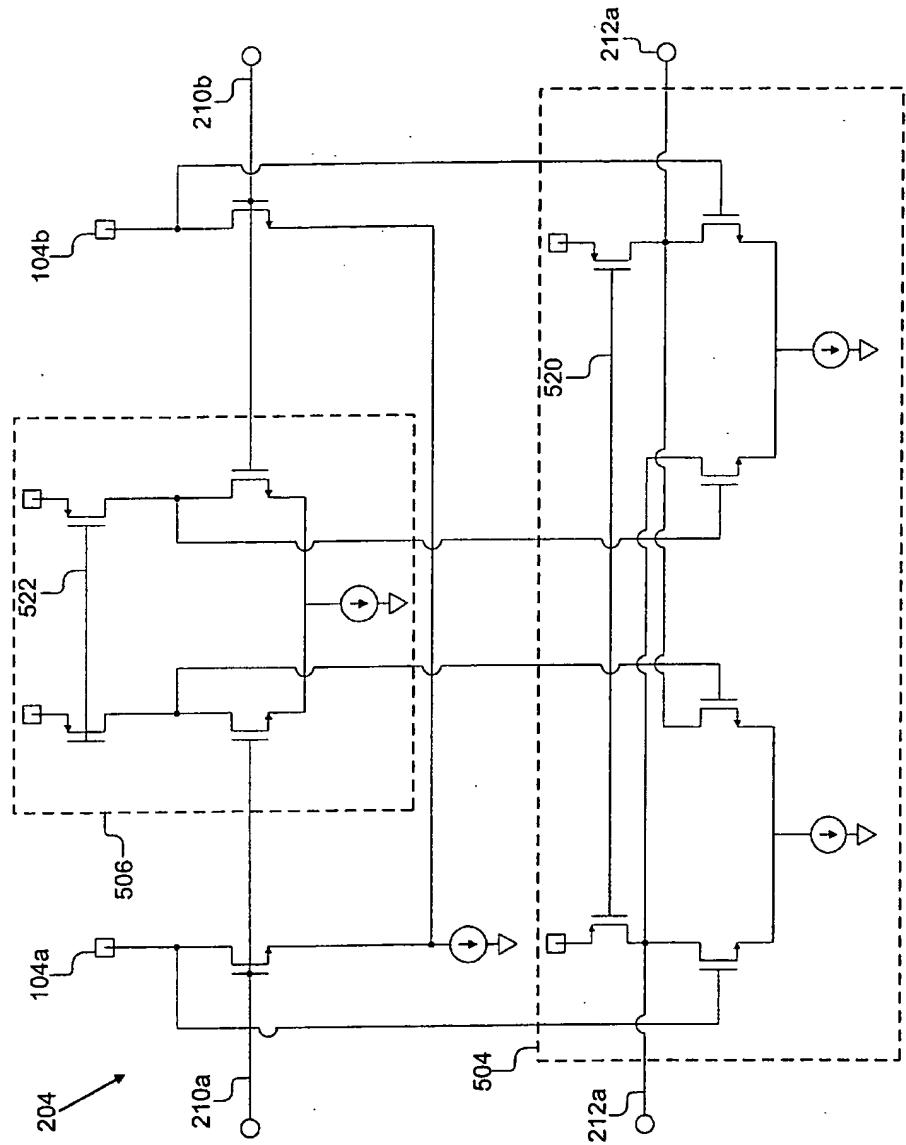


Figure 5B

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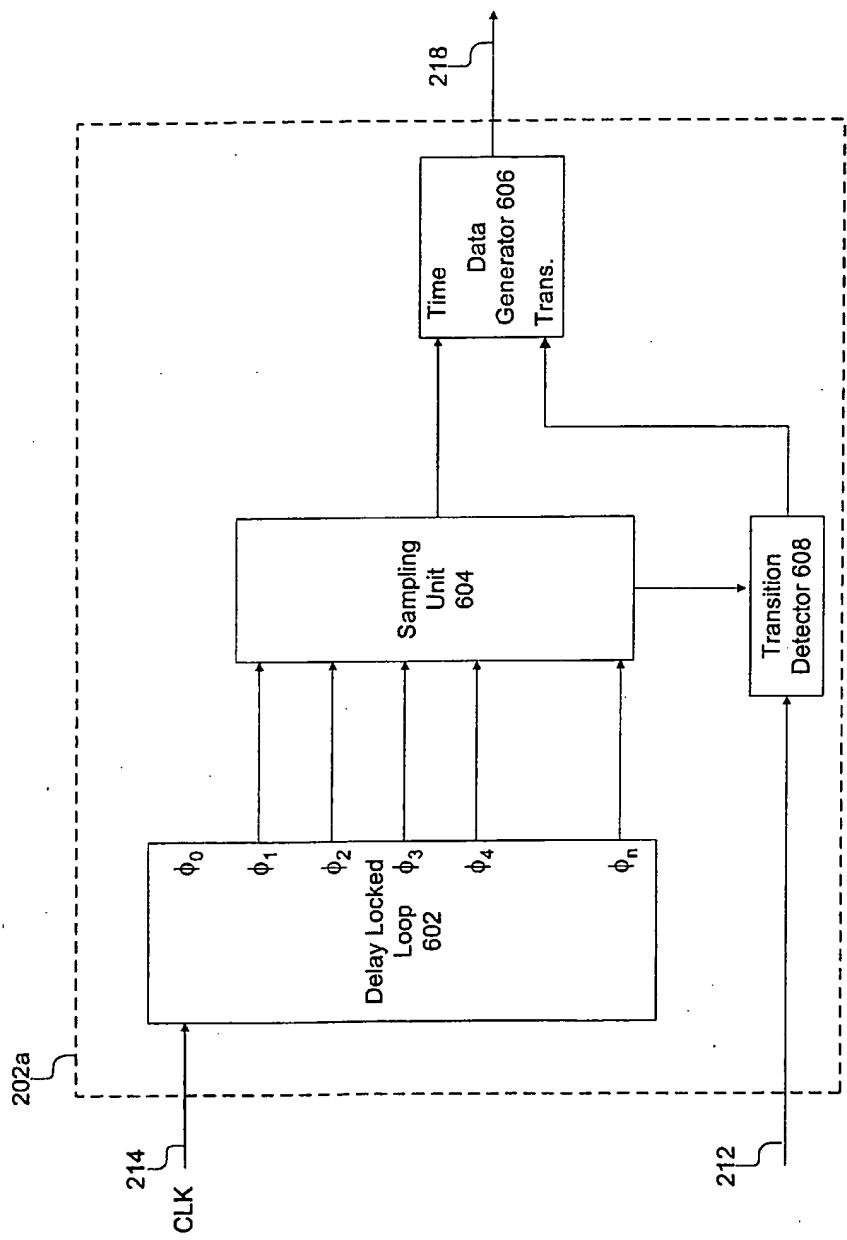


Figure 6A

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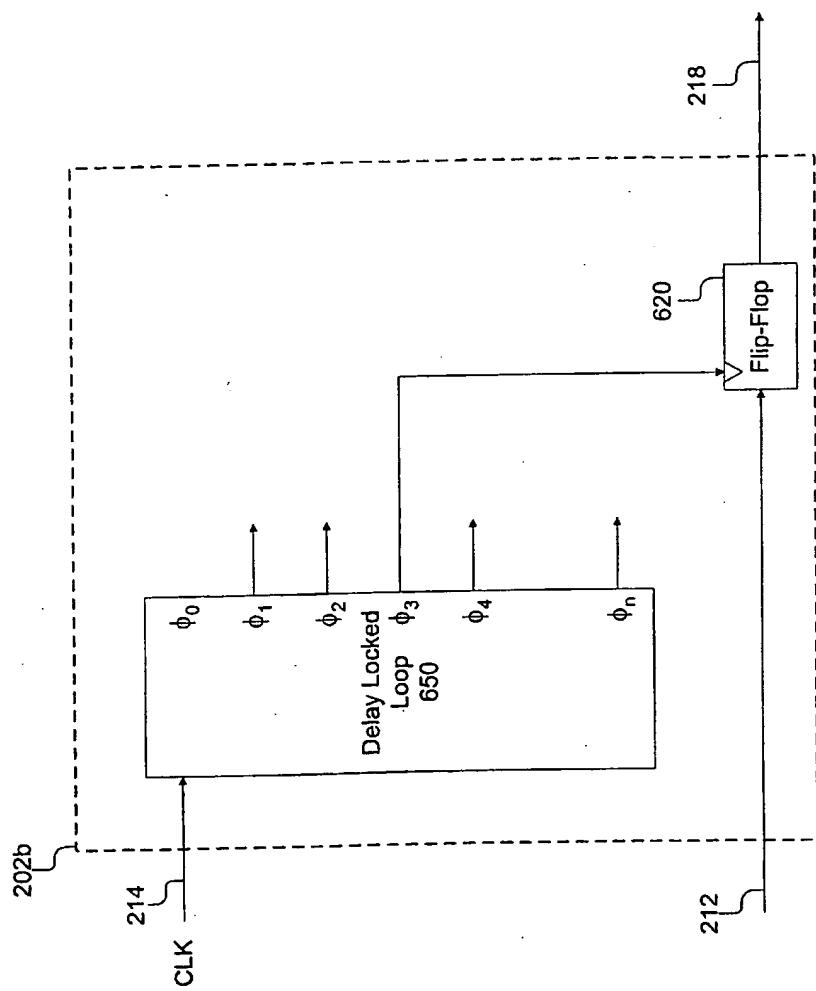


Figure 6B

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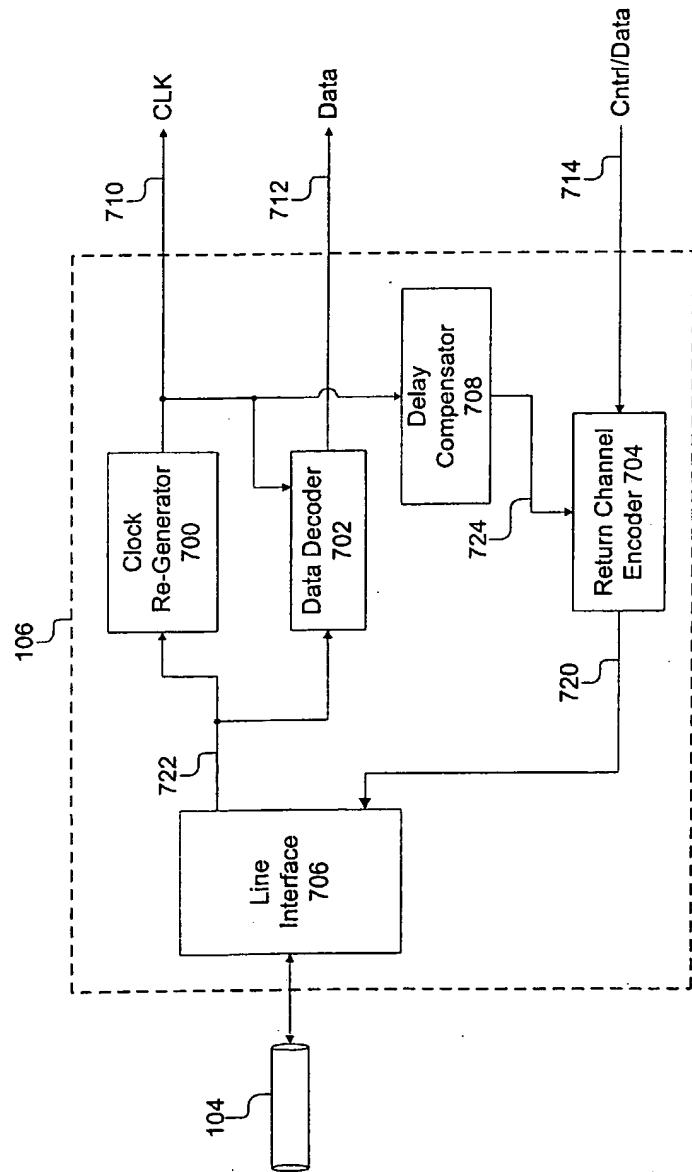


Figure 7

10/17

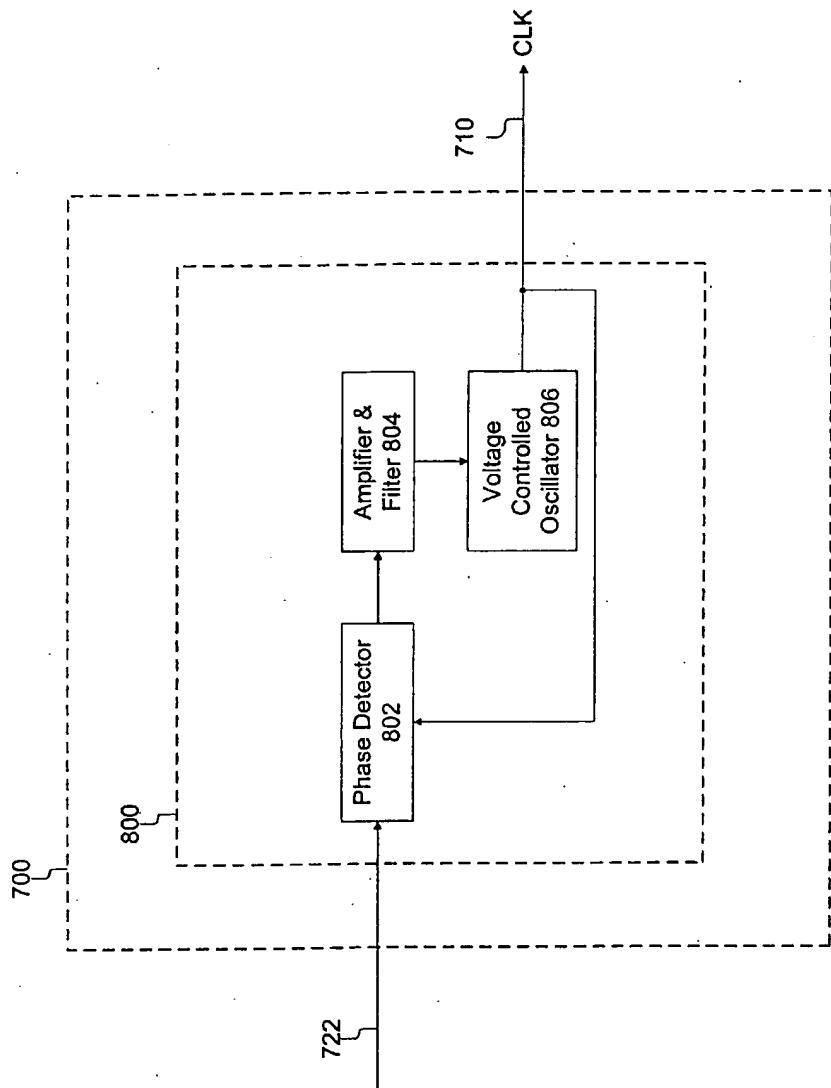


Figure 8

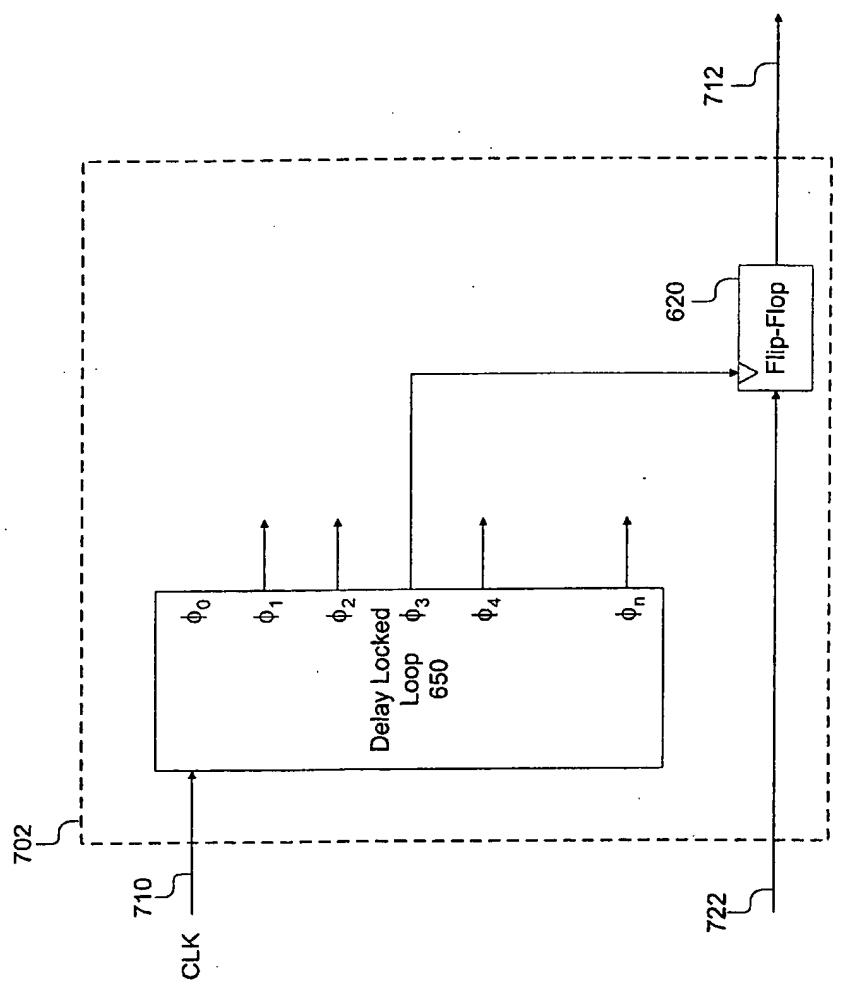


Figure 9

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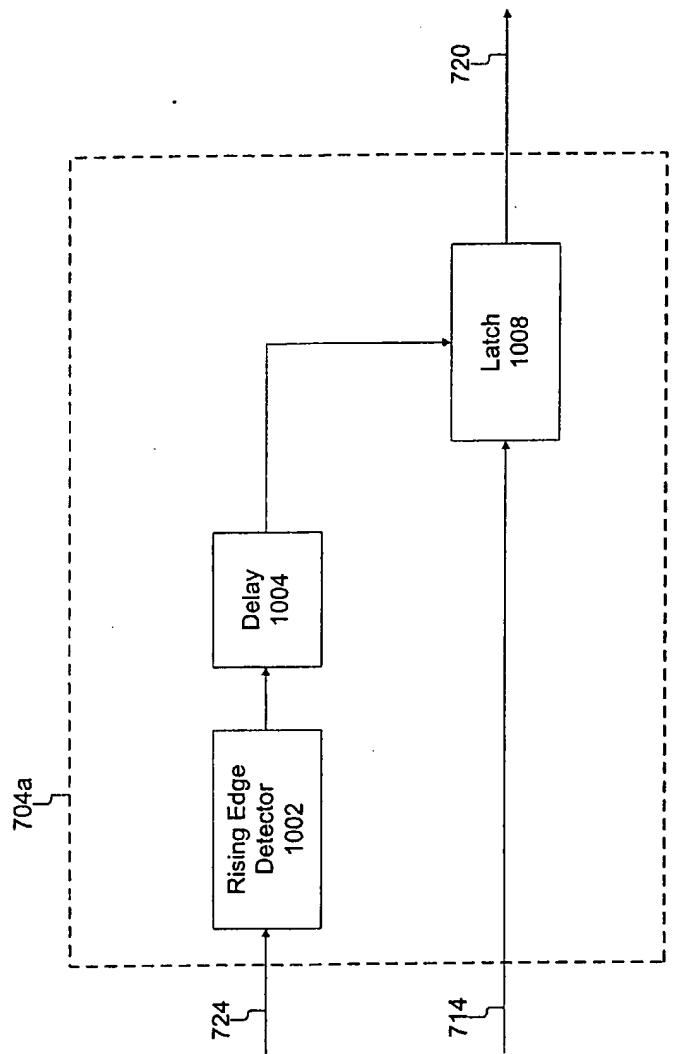


Figure 10A

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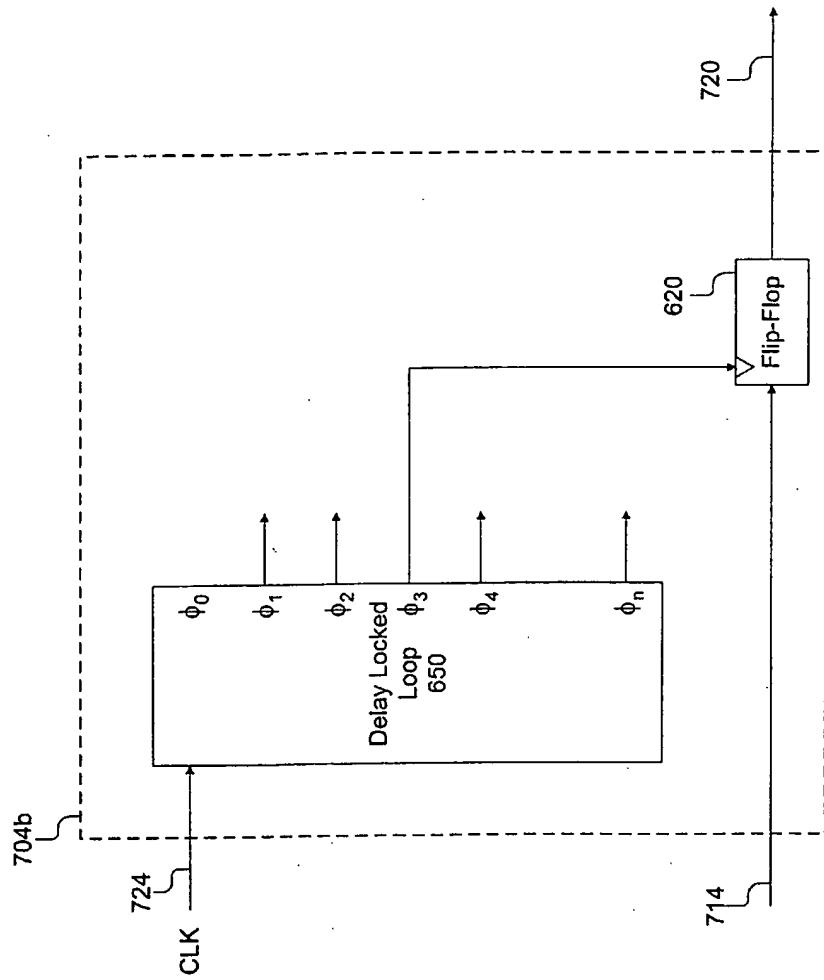


Figure 10B

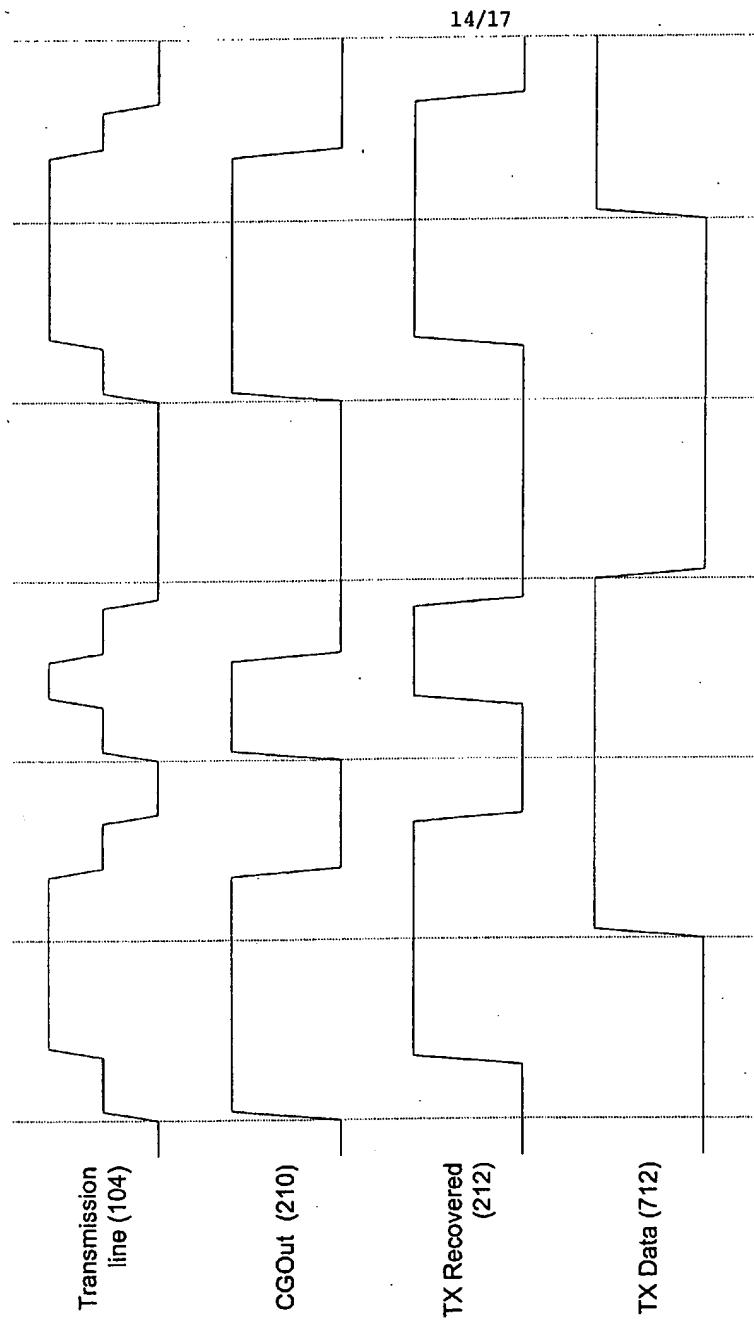


Figure 11A

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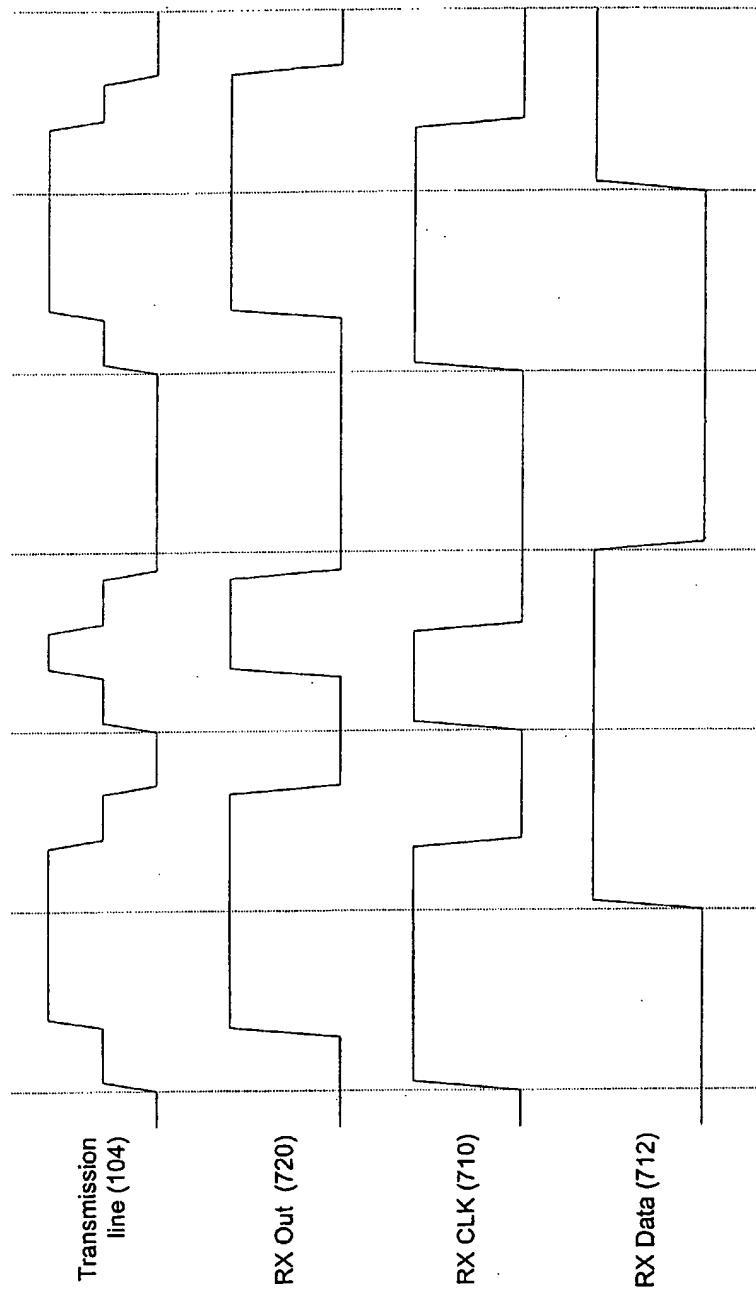


Figure 11B

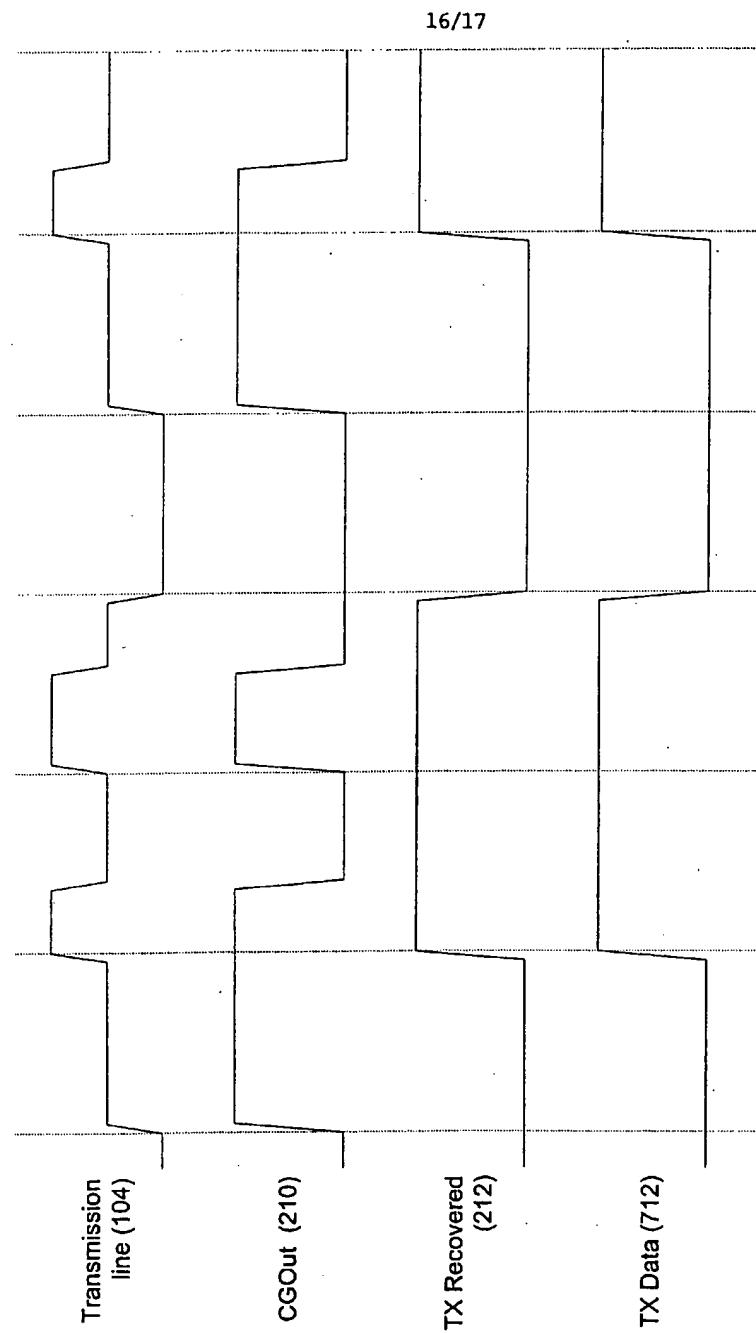


Figure 12A

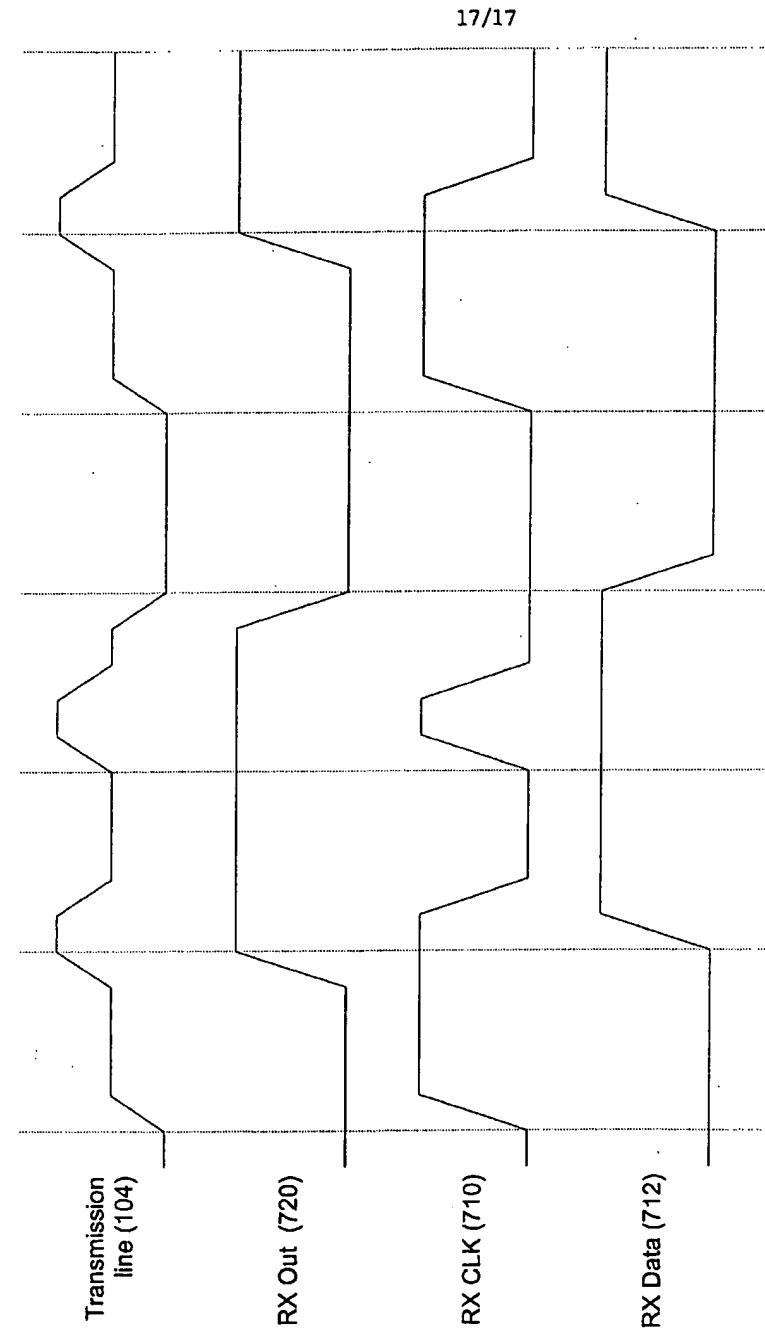


Figure 12B

INTERNATIONAL SEARCH REPORT

Inte .onal Application No	
PCT/US 99/20488	

A. CLASSIFICATION OF SUBJECT MATTER		
IPC 7	H04L25/02	H04L25/49

According to International Patent Classification (IPC) or to both national classification and IPC		
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B. FIELDS SEARCHED		
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Minimum documentation searched (classification system followed by classification symbols)		
IPC 7	H04L	

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)		
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C. DOCUMENTS CONSIDERED TO BE RELEVANT		
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Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KAZUTAKA NOGAMI ET AL: "PHASE MODULATION I/O INTERFACE CIRCUIT" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 37, February 1994 (1994-02), pages 108-109, 318, XP000507077 New York, USA ISSN: 0193-6530 left-hand column, paragraph 2 left-hand column, last paragraph right-hand column, paragraph 2 - paragraph 3 figures 2,3	1-15
Y	--- -/-/	16-18

<input checked="" type="checkbox"/>	Further documents are listed in the continuation of box C.
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<input checked="" type="checkbox"/>	Patent family members are listed in annex.
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Date of the actual completion of the international search	Date of mailing of the international search report
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3 February 2000	10/02/2000
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Name and mailing address of the ISA	Authorized officer
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European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Orozco Roura, C
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/20488

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